This paper was originally presented at the Power Electronics Technology Exhibition & Conference, part of PowerSystems World 2005, held October 25-27, 2005, in Baltimore, MD.
To inquire about PowerSystems World 2006, October 24-26, 2006, please contact jcharno@primediabusiness.com or visit the website: www.powersystems.com

FIGURES OF MERIT FOR HIGH-FREQUENCY SWITCHES

S. L. Colino
Vishay Intertechnology, Inc.
Santa Clara, CA
Steve.Colino@Vishay.com

C. P. Schultz
Vicor Corporation
Andover, MA 01810
CSchultz@Vicr.com

ABSTRACT

Defining and evaluating MOSFETs for power switch and rectifier applications can be facilitated by defining and identifying a figure of merit (FOM) for the application in question. The figure of merit used depends entirely on the topology, and circuit conditions. For each MOSFET function in every switching regulator topology, a unique figure of merit can be developed. Some examples used by the writers are provided herein in an effort to provide insight into the switching processes involved when a power MOSFET is turned on and off at very high frequencies.

INTRODUCTION

In designing a dc-to-dc converter, there are numerous MOSFETs available with seemingly similar characteristics. Figures of merit are used to narrow the choices down to a manageable number by only keeping the best few for detailed evaluation. A figure of merit is usually defined as a parameter or combination of parameters that characterize the anticipated level of performance of a device. Developing a figure of merit involves identifying key parameters pertinent to the application, providing a weighting for each one, and combining them together to form a ranking. In the case of semiconductor physics, for example, a typical figure of merit has always been the mobility of the charge carriers. For example, in silicon semiconductors, electrons have a mobility of 0.135 m/s per V/m where mobility measures the drift velocity the electron acquires per unit applied electric field. Holes in silicon have a lower mobility on the order of 0.049 m/s per V/m. In a field-effect transistor then, an n-channel device, in which electrons are the majority carriers, usually outperforms the corresponding p-channel device, where holes are the majority carriers. Similarly in comparing semiconductor materials, diamond and/or silicon carbide would scale as a higher performing MOSFET than would a gallium arsenide MOSFET, which in turn should be superior to silicon. This argument is made based on the mobility of the carriers in the material. Of course cost, availability, and various processing challenges have plagued every material other than silicon, which remains, at least for the near term, the semiconductor material of choice. The higher the mobility the better, so this figure of merit falls in line with the historical way of defining a figure of merit, i.e. the larger the number the better. Today figures of merit for MOSFETs are conveniently inverted so that the lower the number, the better the presumed performance. This newer convention will be adopted here as well.

For MOSFET manufacturers a key figure of merit (FOM) used in the early 1990s was the **specific rDS(on)** which is the product of the rDS(on) and the active area of the die. For a given process this FOM should be essentially constant regardless of chip size, so that if the chip area from a given design or process is doubled to fit a larger package, the $r_{DS(on)}$ would halve, i.e. the **specific $r_{DS(on)}$** is design and process dependent but is independent of chip area (to first order). An advantage of this figure of merit to a supplier is that for a given $r_{DS(on)}$ target, the die size will be smaller when the specific $r_{DS(on)}$ is lower. A smaller chip size corresponds to better economics of scale (more chips per wafer), which in turn can be split between the consumer and the supplier as a cost reduction. While this was a good figure of merit for low-frequency applications, it did not take the switching capability of the MOSFET into account.

For a dc-to-dc converter operating at high frequency, input capacitance, output capacitance, and gate charge are all relevant in developing a useful figure of merit. The product of $r_{DS(on)}$ and some device capacitance (or effective device capacitance) is usually used for dc-to-dc converters. The product of resistance and capacitance has the units of a time, and the lower RC figure of merit (since less capacitance is also desirable) denotes the higher performance process. This figure of merit also removes the necessity of including die area since resistance decreases inversely and capacitance increases linearly with die size. This product of resistance and a relevant capacitance still measures the goodness of a process because it removes the impact of the physical die size. Table 1 summarizes some recommended figures of merit for use in high-

frequency power switching. Specific applications where these figures of merit would be relevant are also included in the table. Additionally, figure 1 shows some relevant capacitances in a power MOSFET. The reverse transfer capacitance C_{rss} is the feedback capacitance from gate to drain. The input capacitance C_{iss} represents the sum of the gate-source capacitance and the gate-drain capacitance while the device output capacitance, C_{oss}, is the sum of the drain-source and gate-drain capacitance. The total gate charge Q_g is the charge that must be supplied into the gate, at a specified switching condition, to drive the gate from 0 V to some final drive level V_{GS}. The total gate charge is typically divided into three parts, the initial gate-source charge Q_{gs}, the gate-drain charge or Miller charge Q_{gd}, and the overdrive charge. The first two are typically supplied by manufacturers while the overdrive charge can be obtained from a simple subtraction.

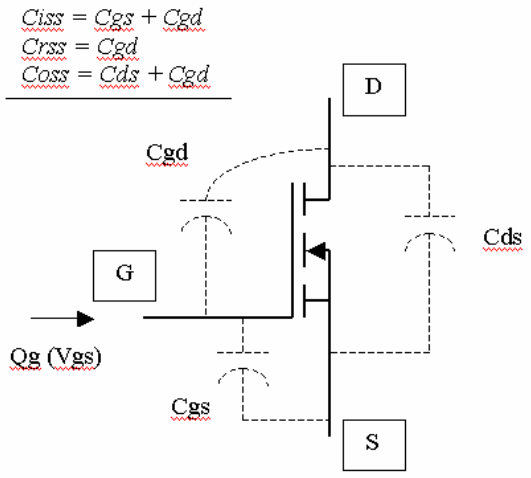


FIGURE 1
MOSFET CAPACITANCES

A brief discussion is in order for each entry in table 1. The mobility used by physicists or semiconductor designers and the specific $r_{DS(on)}$, popular with MOSFET suppliers, have been discussed, as has their benefits. Consider the third figure of merit (FOM) which is the product of the $r_{DS(on)}$ and the total gate charge Q_g required to drive the gate to a specified voltage, V_{GS}, under a specified switching load. The total gate charge relates to the requirement imposed on the driver circuit. This is lost as heat in the V_{cc}/driver circuit and in the gate resistance in the input circuit of the MOSFET and the driver, internal or otherwise. In a dc-to-dc converter the total gate charge times the frequency of operation defines the average current required from the V_{cc} drive supply. When this average current is multiplied by the V_{cc} voltage, the power consumption required to drive the MOSFETs is determined.

$$P_{DRV} = Qg * Vgs * f \qquad (1)$$

Therefore, a figure of merit constructed using the $r_{DS(on)}$ and the total gate charge divided by the applied gate-source drive voltage combines losses in the power train (r_{DS}) and the burden placed on the driver (Q_g). A low $r_{DS} * Q_g/V_{GS}$ figure of merit trades off the ability of the MOSFET to process power in a dc-to-dc converter with the size of the V_{cc} driver circuitry and should signify the most appropriate devices for this application. Utilization of this total gate charge FOM can be relevant in a very high-density power converter. In some applications, the composite driver circuitry may take up as much space as the power FETs.

Table 1 – Some recommended Figures of Merit (FOM) and their usage

FOM	Units	Usage
Carrier mobility μ	Drift velocity per unit E-field	Semiconductor Physics
Specific r_{DS}	Resistance Area	MOSFET manufacturers, low-frequency switching applications
$r_{DS} * Qg/V_{GS}$	Time	Miniaturizing the driver/ minimized Vcc losses
$r_{DS} * Q_{gd}$	Flux	Hard switching
$r_{DS} * \int Crss\ dV$	Flux	Hard switching
$r_{DS} * \{Q_{gd} + \Delta Q_{gs}\}$	Flux	Hard switching
$r_{DS} * Q_{rr}$	Flux	Synchronous Rectifier
$r_{DS} * C_{iss}(V_{DS} = 0)$	Time	Quasi-resonant converter with synchronous freewheeling FET
$\{ r_{DS} * \int C_{oss} * dV \} / Vr$	Time	Zero-current switching (ZCS) applications, particularly offline
$r_{DS} * \int C_{oss} * V\ dV$	Flux * Time	Semi-soft or partial zero-voltage switching (ZVS) applications, particularly offline

It is not necessary to divide the FOM by the actual drive level V_{GS} in the application, however this has the effect of converting the total gate charge into an effective drive capacitance and the resulting FOM has the more familiar units of a time. The remaining figures of merit in table 1 can be divided into hard switching applications and soft switching applications.

HARD SWITCHING

Control Switch

A control switch controls the path of the current. For isolated converters, it is the primary switch; for buck converters, it is commonly referred to as the upper or top switch. Since its function in many isolated topologies is the same as in a buck converter, we will lump these together as a *control switch*. When on, current flows through the control switch, and power dissipation is determined by $r_{DS(on)}$. When off, current follows the rectifier path and power dissipation in the control switch is determined by its leakage (usually negligible). When it is switching, power dissipation is determined by a portion of the Q_g curve, the gate resistance R_g, and in some cases the output charge Q_{oss}. Figure 2 shows the control (Q1) and rectifier (Q2) switches in a single-phase buck converter.

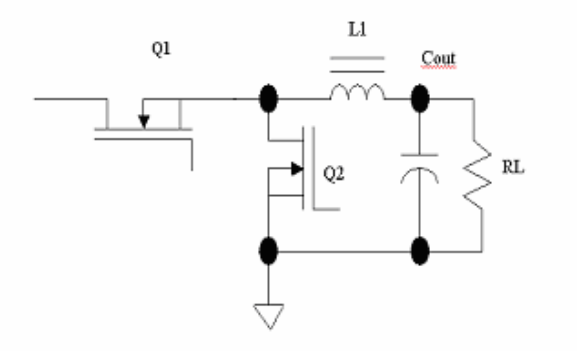


FIGURE 2
SINGLE-PHASE BUCK CONVERTER

Consider the figure of merit associated with the $r_{DS(on)}$ and the Miller charge Q_{gd} (r_{DS}*Q_{gd}). In hard-switched circuits, the MOSFET is turned on and off into a constant load (drain) current and the switching losses are approximately proportional to the transition or crossover time, i.e. the time it takes for the device to turn fully on or fully off. At the all important turn-off event shown in figure 3, drain voltage is transitioned during the Miller portion (Q_{gd}), and the current fall time is determined by the time it takes to discharge the input capacitance of the device (C_{iss}) from its Miller plateau voltage (V_{GS}_pl) to its threshold voltage (V_{GS}_th). Figure 3 is a typically used linear approximation to a hard-switched (constant-current) turn-off. The Miller charge describes the voltage rise time and excludes the current fall time, but the product of $r_{DS(on)}$ and Miller charge Q_{gd} nevertheless represents an often used figure of merit for hard switching and quantifies the ease with which a given driver can turn the device on and off so as to minimize overall losses. To account for the current fall time, the additional charge (ΔQ_{gs}), required to drive the gate from V_{GS}_pl down to V_{GS}_th, can be added to capture the true FOM for this application which is r_{DS} * (Q_{gd} + ΔQ_{gs}). During the Miller interval, the gate-source voltage is essentially fixed, and all of the gate driver current flows through C_{rss} (C_{gd}) with no net current flow into the gate-source capacitance (C_{gs}). At time t=0 (the beginning of the Miller period at turn-off), the voltage across C_{rss} is V_{GS}_pl, where V_{GS}_pl is the gate voltage required to sustain the required drain current. The drain is an $r_{DS(on)}$ drop above the source which is approximately zero. At the end of the Miller portion, the drain has switched from zero to the applied off voltage Vr, but the gate remains at V_{GS}_pl. Therefore the voltage on Crss = Cg – Cd at the very end of the Miller portion equals V_{GS}_pl - Vr. Since all the charge in the driver circuit goes into discharging Crss, the charge transfer integral can be used to determine the charge required from the driver. Therefore a related figure of merit in hard switching is:

$$FOM = r_{DS} * \int_{VGS\_pl}^{V_{GS}\_pl - Vr} Crss(V)\, dV \qquad (2)$$

Yet another variation in the hard-switched figure of merit is to actually integrate the reverse transfer (gate-drain) capacitance, C_{rss}, versus the applied voltage across it between the limits used in the application.

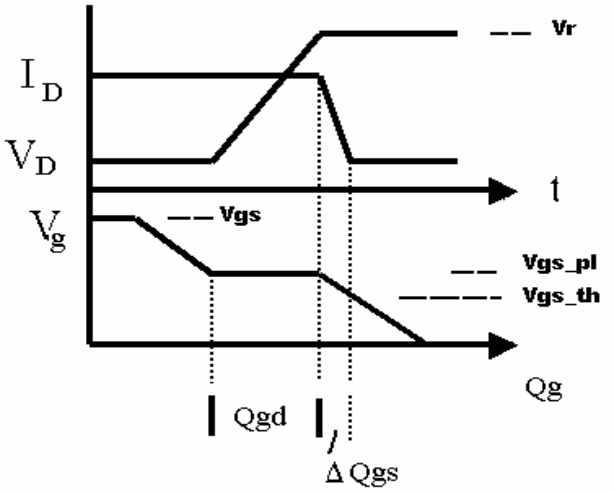


FIGURE 3
LINEAR APPROXIMATION OF SWITCHED WAVEFORMS AT TURN-OFF

An advantage of this integral form of the Q_{gd} figure of merit is that it can be applied at any switched current and switched voltage which may not be identical to that found in the datasheet. Usually the lower limit in (2) can be approximated as zero. Although the Miller charge integral of (2) appears to require a cumbersome numerical integral, the reader is referred to [1] for a closed-form solution provided that the reverse transfer capacitance follows the classical form under reverse bias where:

$$Crss(V) = Co + \frac{Cjo}{(1 + |V| / Vj)^{m}} \qquad (3)$$

where the absolute value allows for the fact that V < 0 during "reverse bias." Substitution of (3) into (2) is straightforward, and with a lower limit of zero, equals:

$$FOM \approx r_{DS} \cdot \{Co \cdot Vr + \frac{Cjo}{(1-m)} \cdot Vr \cdot [(1 + \frac{Vr}{Vj})^{1-m} - 1]\} \qquad (4)$$

The challenge for MOSFET manufacturers is to drive down the Figure of Merit, while at the same time reducing size and cost. Figure 4 is a typical trench FET structure.

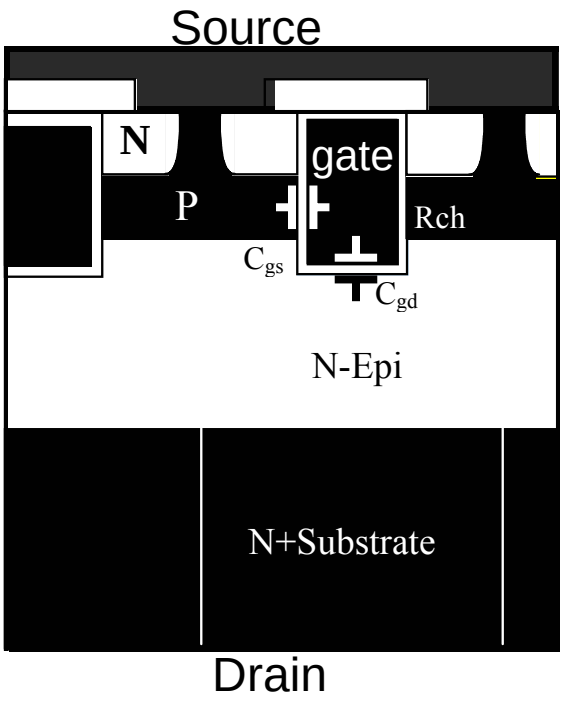


FIGURE 4
TYPICAL TRENCH FET STRUCTURE

The $r_{DS(on)}$ is comprised of package, substrate, epi, and channel (R_{ch}) resistances. Package resistance has been driven down by bondwireless packages, such as the Vishay Siliconix PolarPAK™ shown in figure 5. The die is connected directly to the leadframe prior to encapsulation, eliminating any need for wirebonds and their excess resistance and inductance. Substrate resistance has been reduced by the utilization of thinner substrates. The limitation on substrate thickness is its fragility. Epi resistance in low-voltage-rated MOSFETs has not been the subject of much reduction.

Of all the components of resistance that have been addressed, the most significant in low-voltage devices remains the channel resistance. Advanced processing in recent years has allowed the cell density of a trench gated MOSFET to increase from 8M cells per square inch to 287M today. One of the process difficulties is to reduce the feature sizes of the gates to drive down C_{gs} and C_{gd}. Through lateral scaling, C_{gd} has been kept under control, and through vertical scaling, C_{gs} has been kept under control. In addition, with WFET®, Vishay has been able to further reduce C_{gd} with a negligible impact on $r_{DS(on)}$.

FIGURE 5
EXAMPLE BONDWIRELESS PACKAGE

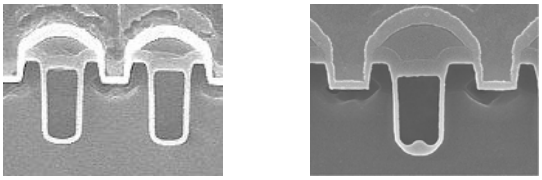


FIGURE 6
TYPICAL WFET CROSS SECTION

The net effect has been a dramatic increase in performance in hard switched dc-to-dc conversion due to a continual decrease in $r_{DS} * Q_{gd}$, a trend which is summarized in table 2.

TABLE 2 - TYPICAL 30-V DEVICE IMPROVEMENT IN HARD-SWITCHED FOM

Part Number	V_{DS}	V_{GS}	R4_5	Q_{gd}	FOM
Si4324DY (WFET)	30	20	0.0042	6.6	27.72
Si4336DY	30	20	0.0042	10	42.00
Si4856ADY	30	20	0.0076	7.2	54.72
Si4406DY	30	20	0.0055	10	55.00
Si4856DY	30	20	0.0085	7.2	61.20
Si4892DY	30	20	0.02	3.5	70.00
Si4410DY	30	20	0.02	7	140.0

The products $r_{DS}*Q_{gd}$, $r_{DS}*(Q_{gd} + \Delta Q_{gs})$, plus the integral form in (4) are all figures of merit which are independent of die area since r_{DS} is inversely proportional to die area and gate charge/capacitance is proportional to die area. It produces a balance between on-state and switching capabilities. Once a good process is determined, the die has to be sized, and other

tradeoffs, such as area for gate fingers to lower Rg, or varying the gate to source threshold voltage, have to be made for specific duty cycle, gate drive, and load current conditions. As the basic figure of merit dramatically decreases, these parameters, which used to be ignored, must be accounted for in the design of the MOSFET and are also important in MOSFET selection.

Rectifier Switch

Of concern in the synchronous rectifier switch, Q2, is its on-state conduction loss, which becomes particularly significant at low output and/or high input voltages where the RMS (Root Mean Square) current is high.

$$P_{cond} = I_{RMS}^2 * R_{DSON} \qquad (5)$$

The same methods used to drive down $r_{DS(on)}$ in the control switch apply to the rectifier switch. However, the benefit of low Q_{gd} is different.

Low Q_{gd} and low C_{rss} are additionally relevant in the rectifier switch since the tendency for spurious dV/dt turn-on [4] of the rectifier switch is reduced. A reapplied drain dV/dt at turn-off will couple a current into the MOSFET gate through C_{gd}, attempting to turn the device back on. For a given dV/dt, lower C_{gd} results in less dV/dt-generated current, lessening the tendency for spurious turn-on. However as Q_{gd}, C_{gd}, and R_g are decreased, the control switch will turn on faster, which further increases the need for smaller feedback current to the gate of the rectifier switch. A MOSFET parameter for good dV/dt immunity is a low ratio of Q_{gd}/Q_{gs}. During the dV/dt event, Q_{gd} attempts to drive the gate on, while Q_{gs} tries to hold the gate off. The absolute dV/dt boundary of V_{GS} for the buck converter rectifier switch is given by:

$$V_{GS} = V_{IN} \int_0^{Vin} \frac{Crss}{Ciss} dV \qquad (6)$$

This assumes that no current is drawn out of the gate by the gate drive during the dV/dt event. As V_{GS} increases, some charge is removed from C_{gs} through R_g and the drive resistance to ground, but as long as V_{GS} stays below the point where the rectifier switch begins to conduct significant current, it will be immune to the dV/dt. It is important to distinguish significant current from current at V_{GS}_th which is typically defined by 250 µA. For the Si7336ADP, the minimum V_{GS}_th is 1 V (see figure 7) but significant current flows only at V_{GS} = 2.8 V at 25 °C, and 2.4 V at 125 °C.

A parametric estimate for dV/dt immunity is:

$$Q_{ratio} = \frac{Q_{gd}}{Q_{gs} + Q_{gd}} \qquad (7)$$

Q_{ratio} is independent of die size and cannot be directly combined with $r_{DS(on)}$ to form a figure of merit since the result would be dependent on die size.

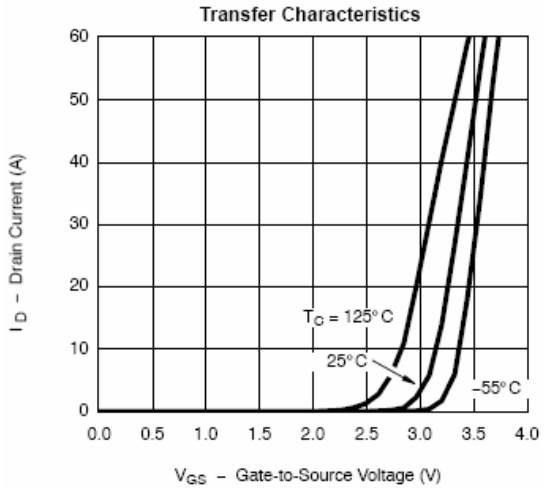


FIGURE 7
Si7336ADP TRANSFER CHARACTERISTICS

Other complications can occur at Q2 turn-off if there is still residual stored charge in the junction region of body drain diode, i.e. if the body diode conducted at any time and its stored minority carrier charge was not completely removed. If FET Q1 should turn on while FET Q2 is unable to block voltage because of reverse recovery phenomena in its body diode, the Q1/Q2 pair provides a current path as shown by the arrow in figure 8, which constitutes a direct short across the input.

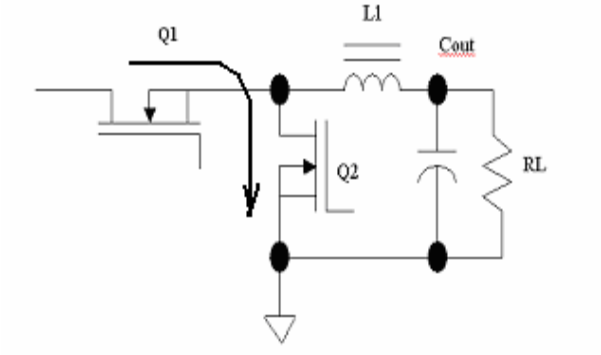


FIGURE 8 – UNWANTED BUCK CONVERTER CURRENT PATH

Current shoot-through would be limited by intrinsic resistance/inductance in this path and by the properties of the MOSFETs themselves and can lower efficiency. Should issues arise related to Q2's body diode conduction, the ability of Q2 to quickly block voltage

would be a strong function of the reverse recovery charge, Q_{rr} and the snappiness of the body diode's recovery. Usually for low-voltage MOSFETs, this problem is easily manageable but in certain types of active clamp reset circuits using higher voltage rated MOSFETs, the complications are usually more severe.

When the control switch Q1 is turned off, current will commutate through the rectifier switch, regardless of whether it is turned on or not. Very often, Q2 is turned on while current flows through its body diode, and the drain-to-source voltage is nearly zero, resulting in Q2 being zero voltage switched at turn-on. This reduces Q2 turn-on losses to nearly zero. When MOSFET Q2's channel starts to conduct, its $r_{DS(on)}$ shunts its body diode and the body diode current offloads to the MOSFET channel. How effective the channel is in diverting body diode current depends in part on the $r_{DS(on)}$ drop. A 2-mΩ MOSFET channel conducting 50 A drops 100 mV which is much less than a forward diode drop and in this case the channel would be effective in diverting the body diode current (parasitic circuit inductance notwithstanding). A 20-mΩ $r_{DS(on)}$ MOSFET, in conducting the same 50 A, would drop 1 V and the channel would be much less effective at shunting the body diode. Therefore in some cases where sufficient care is not exercised, the reverse recovery of Q2's body diode results in unwanted power dissipation and in extreme cases can lead to device failure. Q_{rr} is a function of the junction volume of the body diode, and the current. As cell density has increased, the percentage of the die having the p/n junction has decreased, further lowering Q_{rr} providing another advantage. The excess dissipation is given by:

$$P_{rr} = \alpha * Q_{rr} * V_{IN} * f \qquad (8)$$

where α describes the portion of Q_{rr} related to recovery of the diode's reverse blocking capability but must also account for any removal of stored charge by the channel. Considering dV/dt immunity separately, a rectifier switch figure of merit would be limited to the parameters that directly contribute to power dissipation and a suitable FOM in this case might be $r_{DS} * Q_{rr}$. The r_{DS} is inversely proportional to die size and Q_{rr} is directly proportional to die size so this figure of merit is independent of die size. Some devices exhibiting a low $r_{DS(on)} * Q_{rr}$ figure of merit are compiled in table 3. The quantity $r_{DS(on)} * Q_{rr} * Q_{ratio}$ may also be a relevant figure of merit to use in some rectifier applications.

SOFT SWITCHING

Soft switching applications have a very unique set of FOMs. Consider the quasi-resonant forward converter with an active clamp reset and synchronous rectification. Figure 9 is an isolated QR topology with the synchronous rectification shown only in the freewheeling rectifier for simplicity. It will now be shown that this rectifier is naturally zero voltage switched (ZVS) at BOTH turn-on and turn-off without any extra circuitry required. To see this, consider the ON time of the high-side main switch Q1. Prior to Q1 conduction, the freewheeling synch FET Q2 is circulating current through L1 to the load R_L with its gate voltage pre-charged to some positive drive level commensurate with an n-channel enhancement mode MOSFET.

TABLE 3 - LOW $r_{DS(on)} * Q_{rr}$ DEVICES

Part No	V_{DS}	R4_5 max	Q_{rr}	Q_{ratio}	FOM	Package	V_{th} min
Si7868ADP	20	2.75	43	0.48	118	PPAK SO-8	0.6
Si7108DN	20	6.1	20	0.44	122	PPAK 1212	1.0
Si7866ADP	20	3.0	41	0.45	123	PPAK SO-8	0.8
Si4304DY	30	3.7	40	0.42	148	SO-8	0.6
Si7356ADP	30	4.0	40	0.43	160	PPAK SO-8	1.0
Si4324DY (WFET)	30	4.2	40	0.36	168	SO-8	1.4
Si7668ADP (WFET)	30	3.4	51	0.36	173	PPAK SO-8	0.6
Si7104DN	12	3.7	49	0.49	181	PPAK 1212	0.6
Si7380ADP	30	3.5	52	0.36	182	PPAK SO-8	0.6

The voltage at Q2 drain is an $r_{DS(on)}$ drop below the output return when Q2 conducts. When main switch Q1 turns on, the leakage inductance in transformer T1 forms an under-damped circuit with the resonant capacitor C_{res} in the secondary, causing the voltage at the drain of rectifier FET Q2 to ring up to twice the reflected primary winding voltage. Q1's ON time is chosen to approximately equal the time it takes for the current in the series rectifier D1 to reach zero (zero current switching, ZCS). However with main switch Q1 turned on and synchronous rectifier Q2 turned off, the relatively large resonant capacitor causes the voltage at the drain of Q2 to rise very slowly in much the same way that a capacitive snubber limits MOSFET dV/dt.

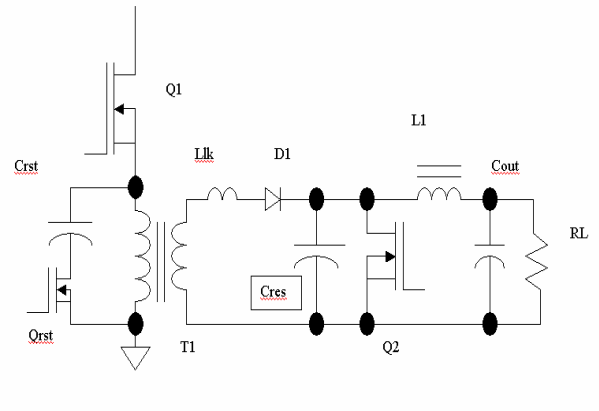


FIGURE 9
QUASI RESONANT FORWARD WITH ACTIVE CLAMP RESET IN THE PRIMARY

For even moderate speed turn-off, device Q2 is easily zero voltage switched at turn-off. This is shown in the waveform of figure 10 which represents a 3.3-V output dc-to-dc converter using a 30-V synch FET, Si7856DP. The uppermost waveform represents the source voltage of main FET Q1 (also equal to the primary winding voltage of T1) and is included here for timing purposes, while the resonant capacitor voltage on the secondary side (also the drain of the synch FET Q2) is provided in channel 2 just below the Q1 source trace. Channel 3 at the bottom is the Q2 gate waveform. By comparing the synch FET gate and synch FET drain (C_{res}), it is clear that Q2 is zero voltage switched at turn-off, and occurs at the point in time indicated by the arrow.

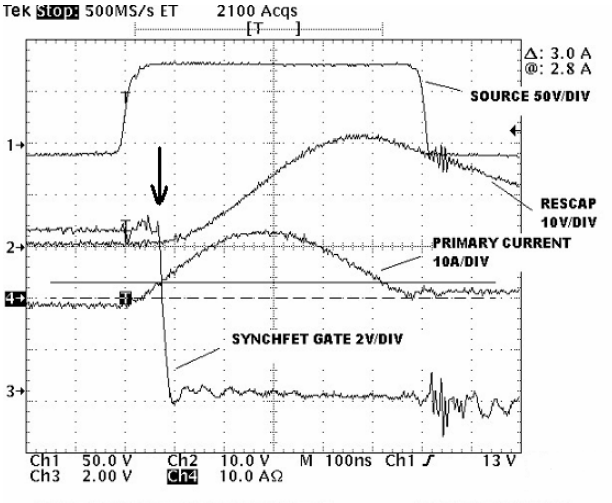


FIGURE 10
Q2 SYNCH FET TURN-OFF AT HLFL

Having demonstrated that Q2 is zero voltage switched at turn-off, we consider next the turn-on sequence for synch FET Q2. At the end of the resonant on period, main switch Q1 turns off at which time the resonant capacitor C_{res} is roughly "peak" charged to its full value of twice T1's reflected primary voltage. As the secondary winding voltage of T1 collapses, series rectifier D1 is reverse biased by the positive voltage present at its cathode. Synchronous rectifier Q2 is not driven on at this point and resonant capacitor C_{res} discharges linearly through the output inductor L1 into the load. The linear discharge can be seen on the resonant capacitor waveform in channel 2 of figure 10 at the end of the trace after main switch Q1 has turned off. Eventually resonant capacitor C_{res} is discharged down to 0 V at which time synch FET Q2 is turned on. It is therefore apparent that synch FET Q2 is zero voltage switched at turn-on as well. This event, shown for the same 3.3-V dc-to-dc converter as figure 10, is included as figure 11.

The arrow in this figure represents Q2 turn-on as V_{GS} in channel 3 is driven positive and the resonant capacitor voltage at Q2 drain on channel 2 is approximately 0 V at this transition. Therefore switching losses, aside from power loss in the internal gate resistance of Q2 is effectively reduced to zero. Note that in figures 10 and 11, the gate waveforms are conspicuous with the absence of a Miller effect, since the device is naturally zero voltage switched at BOTH switching transitions and so no Miller effect is observed.

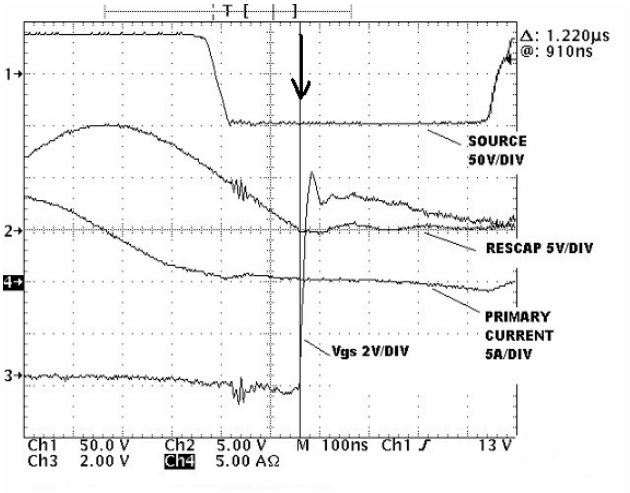


FIGURE 11
Q2 SYNCH FET TURN-ON AT LLFL

Therefore turn-on and turn-off of Q2 is a simple capacitive charging and discharging of its non-linear input capacitance, C_{iss}. Since the drain is not hard switched and $V_{DS} = 0$ at both transitions, C_{iss} at an applied drain bias is no longer relevant and an approximate figure of merit for this application might be $r_{DS(on)} * C_{iss}$ @ $V_{DS} = 0$, where the zero bias value of C_{iss} is typically provided in supplier capacitance curves. In reality, $C_{iss}(0)$ represents only part of the input capacitance. Throughout both transitions, V_{DS} may equal zero, but as the gate is charged up to a level V_{GS}, the input capacitance $C_{iss} = C_{gs} + C_{gd}$ is charged to V_{GS} as well but in a polarity opposite that normally provided in supplier curves of C_{iss} versus reverse drain bias. A more appropriate figure of merit might be:

$$r_{DS} * \int_{0}^{-V_{GS}} C_{iss}(V)\, dV \approx r_{DS} * C_{iss}(0) \qquad (9)$$

A positive polarity on a limit of integration merely signifies that the polarity of the voltage is the opposite of the usual case of an applied "reverse" drain bias. Typically, the value of C_{iss} at $V_{DS} = 0$ and $V_{GS} > 0$ for an n-channel device is slightly higher than the datasheet value of C_{iss} at $V_{DS} = V_{GS} = 0$. A figure of merit $r_{DS(on)} * C_{iss}(0)$ is a good approximate FOM where $C_{iss}(0)$ can be read from datasheet capacitance curves. The integral in (9) represents charge but the FOM used in (9) can easily be converted into familiar units of time by defining an "effective" capacitance based on the charge

integral divided by the final V_{GS} value.

$$r_{DS(on)} * \frac{1}{V_{GS}} \int_{0}^{-V_{GS}} C_{iss}(V)\, dV \qquad (10)$$

Most of the FOMs discussed up to now have related $r_{DS(on)}$ with a performance attribute of the gate circuit (C_{iss}, C_{rss}, Qg, etc.). For some soft switching applications the output capacitance, C_{oss}, and output charge, Q_{oss}, are significant. This is particularly true with higher voltage rated MOSFETs. Consider the power switch Q1 in the quasi-resonant forward converter shown previously in figure 9. When Q1 turns on, its source is pulled up toward the dc input voltage and the source waveform is polarity inverted relative to the drain voltage when a low-side switch is used. If turn-off of main switch Q1 is made to occur when the secondary current reaches zero (ZCS), turn-off switching losses are effectively negated in the power switch as well. However Q1's output capacitance, C_{oss}, must still be recharged by the stored magnetizing energy of T1. If C_{oss} is too high and/or peak magnetizing current in the first quadrant of the BH curve is too low, the transition of the drain may take a very long time. Stretching out the drain turn-off will lead to higher peak voltages on Q1 as transformer T1 resets and will further cause inefficiencies elsewhere in the circuit. Increased drain ON time leads to higher flux levels in the core increasing core loss and also increasing the conduction loss in the reset switch due to higher peak reset currents. The result is lower dc-to-dc converter efficiency. Figure 12 illustrates the importance of low C_{oss} in this case. The uppermost waveform in channel 2 is the source voltage of high-side switch Q1 when the input voltage of a particular offline dc-to-dc converter is 250 V. When Q1 is on, the source voltage is pulled up within an $r_{DS(on)}$ drop of the dc input voltage. At turn-off, the source of Q1 (also equaling the primary voltage of T1) is pulled negative as the core of T1 resets. The bottom waveform of channel 3 is a particular internal control signal defining the turn-off instant of the controller with the dashed cursor indicating the controller's assertion of the desired turn-off transition. It takes approximately 170 ns for the drain to reach its final reset voltage (-300 V across the primary winding). For operation at 1 MHz, this represents 17% of one switching period. Even with a very fast gate driver, a ZCS application such as this requires low output capacitance as a desirable MOSFET attribute. The drain rise time (appearing as a fall time of the source waveform in a high side switch configuration) therefore depends on the area underneath the C_{oss} versus V_{DS} curve in this ZCS application. For example at the turn-off instant, the drain-source voltage is an $r_{DS(on)}$ drop which is approximately 0.5 V for figure 12. When the device reaches the final reset voltage, the reapplied drain-source bias is about V_r = 550 V (250-V dc input + 300-V T1 reset). Therefore integrating the capacitance curve between 0.5 V and 550 V provides the output charge required to completely transition the drain. The criticality of low output charge, in this example, would make the area under the C_{oss} curve a parameter in an FOM.

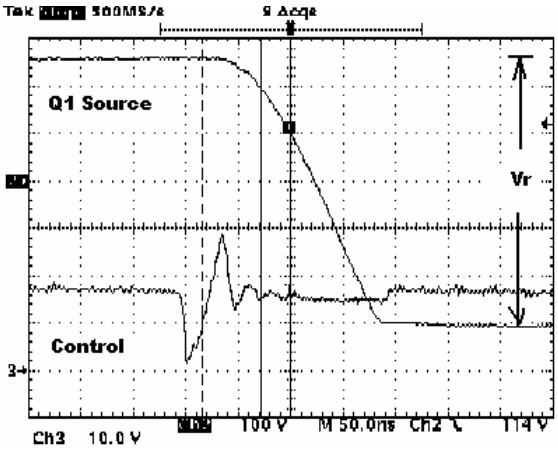


FIGURE 12
ZCS TURN-OFF TRANSITIONS IN AN OFFLINE CONVERTER

Therefore an appropriate figure of merit might be:

$$r_{DS(on)} * \frac{1}{Vr} \int_{0}^{Vr} C_{oss}(V)\, dV \qquad (11)$$

The integral in (11) is the output charge, Q_{oss}, of the FET from 0 to V_r. Division by V_r, the final reapplied drain-source reverse bias, merely adjusts the units of the FOM to a time and converts the charge transfer integral into an "effective" output capacitance. As an aside, note from figure 12 that turn-off of main FET Q1 occurs at both zero load current (ZCS) and at zero voltage (ZVS) so this transition virtually negates turn-off losses. ZVS naturally follows ZCS because the gate driver can sink high current, and turns the channel off long before the drain voltage has a chance to significantly increase.

Another application where output capacitance is relevant is the very same power switch Q1 but at turn-on. Zero voltage switching can be accomplished at turn-on by using the energy stored in the core when it operates in the third quadrant of the BH curve. Reversal of magnetizing current in an active clamp reset dissipatively discharges Q1's output capacitance prior to Q1 turn-on [3] (a suitable delay between reset switch turn-off and Q1 turn-on is required). In some cases at high operating frequencies, it may be more practical to use partial ZVS at turn-on rather than the full ZVS. At least one reason is due to the fact that if the Q1 source voltage of figure 9 rises above 0 V, T1 primary has a

positive primary winding voltage and energy can be transferred through the secondary. While this is desirable, it may produce other complications. The additional dead time introduced into the circuit by increasing the delay time between power and reset switch can also produce other inefficiencies when operating at high frequencies above 1 MHz. The result is that only a percentage of the total drain voltage swing is "hard switched" and dissipated in the MOSFET. However it is not "hard switched" in the usual sense of the word. Figure 13 shows a typical partial ZVS event at turn-on of the high side main switch Q1. The bottom waveform is the Q1 source voltage showing the turn-on event of Q1 during this new type of "semi-soft" switching.

The ZVS interval where both switches are off is indicated and equals the delay time between turn-off of the reset device Q_{rst} and turn-on of the main switch Q1. During the ZVS interval, neither primary-side switch (main or reset) conducts and magnetizing current flows in the primary winding of T1 in a direction such that positive current flows into the source of Q1 back toward the dc input voltage source. As Q_{rst} and Q1 are off, the third quadrant magnetizing energy acts to non-dissipatively discharge the output capacitance of Q1 (and recharge Q_{rst}). However ZVS is incomplete in this case, and the "hard switched" portion of the drain voltage, Va, is indicated in the figure as "turn-on loss." The transition instant between the non-dissipative ZVS and the hard switching is clearly seen by the rapid break in the dV/dt on the leading edge of the Q1 source waveform in figure 13. This is the only switching loss element in the power switch, since we have previously demonstrated that the turn-off event of Q1 is BOTH zero voltage and zero current switched (zero reflected secondary current).

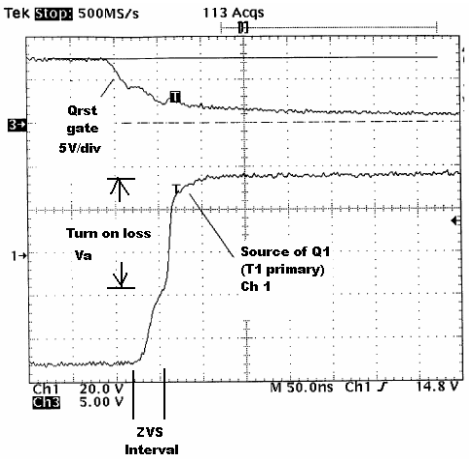


FIGURE 13
PARTIAL ZVS (SEMISOFT SWITCHING)

The topmost waveform in figure 13 is the gate waveform of the active clamp reset switch, included to demonstrate timing. It will now be shown that the aforementioned switching energy dissipated in main switch Q1 at turn-on equals the energy integral of the output capacitance. To do this, we must first demonstrate the absence of a crossover power dissipation term at turn-on, which can only be the case if Q1 is turned on at zero reflected load current (since full ZVS is not realized). Just prior to Q1 turning on, freewheeling current flows through synch FET Q2, L1, and to the load. There is no current flow through Llk (secondary referenced leakage inductance of T1) just prior to Q1 turn-on. When Q1 turns on, the reflected primary voltage appears across Llk and ramps up the secondary current in the leakage inductor. Because the leakage inductance is made intentionally larger than a normal parasitic leakage (to resonate with the resonant capacitor C_{res}), the secondary current begins to build up "relatively" slowly. Therefore Q1 also turns on at zero current because the leakage inductance is large enough to limit turn-on di/dt similar in many ways to an external inductive turn-on snubber. Therefore with no load current and no crossover power dissipation at Q1 turn-on, the hard-switched energy that is dissipated in the MOSFET would be the same as the energy required to discharge C_{oss} from an initial value, Va, to 0 V. This stored capacitive energy on C_{oss} is internally dissipated within Q1, and a relevant figure of merit in this case might be:

$$r_{DS(on)} * \int_0^{Va} C_{oss}(V) * V * dV \qquad (12)$$

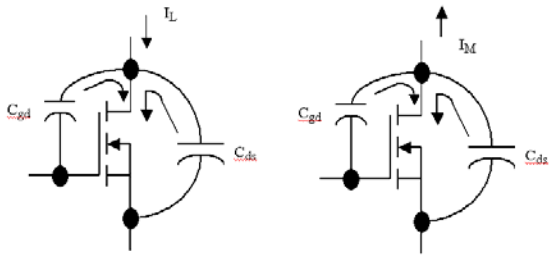
where Va is defined per figure 13. The units of this FOM are resistance times energy, but this can easily be converted to a time by defining an effective capacitance, Coss_eff, based on an equivalent linear capacitor, which would have the same stored energy at Va as would the energy integral given in (12).

$$\tfrac{1}{2} (Coss\_eff)\, V_a^2 = \int_0^{V_a} Coss(V) * V * dV \qquad (13)$$

Although the output charge integral of (11) and the energy integral in (12) appear to require numerical solutions, the reader is referred to [1] for a closed form solution to both integrals provided that the output capacitance follows the classical form of (3).

The energy integral represents the minimum switching loss that can ever be achieved in a hard switched circuit and is solely a function of the MOSFET's output capacitance C_{oss}. This is illustrated in figure 14a where a "load" current I_L is hard switched in the drain. In this case it is clear that the displacement energy stored in the output capacitance is additive with the crossover or transition energy introduced by hard switching the load current.
However, in a semi-soft switching active clamp reset

circuit such as that of figure 9, turn-on of Q1 occurs when the power transformer operates in its third quadrant and magnetizing current I_M flows in a direction from source to drain. Therefore in practice, there is crossover power dissipation in Q1 at device turn-on since MOSFET Q1 must still hard switch T1's magnetizing current, which is smaller in magnitude but nevertheless is still non-zero.



(a) (b)

FIGURE 14
STORED FET ENERGY FLOW & LOAD CURRENT FLOW DURING HARD/SOFT SWITCHING

This phasing of the MOSFET's output displacement current and the external magnetizing load current is important in understanding the relevance of the energy integral in (12). Figure 14b illustrates this case. The discharge current of the FET's output capacitance is in phase with the direction of the magnetizing load current. Therefore the energy integral derived FOM will correspond to a minimum switching loss in a hard-switched application and to the case where the switched drain current is sufficiently low. In the case where ZVS is achieved through magnetizing current reversal and where I_M is not low enough to be neglected, the losses become a complex combination of how much hard switched transition energy is lost in the FET relative to the energy stored on C_{oss}.

Consider for example a 220-V rated Si7302DN. A fit of the output capacitance C_{oss}, to the function of (), is shown in figure 15. The measured data points are indicated as squares superimposed on the functional fit. In this instance, Co = 12.5 pF, Cjo = 518.1 pF, Vj = 0.184 V, and the exponent m = 0.485. The energy integral in (12) is straightforward using (3) and the closed form solution is:

$$E\_sw = \frac{Cjo \cdot Vj \cdot Va}{(1-m)} \cdot (1+\frac{Va}{Vj})^{(1-m)} + \frac{1}{2} \cdot Co \cdot Va^2 - \frac{Cjo}{(1-m)\cdot(2-m)} \cdot Vj^2 \cdot [(1+\frac{Va}{Vj})^{2-m} - 1] \quad (14)$$

If this device hard switched 100 V with zero load current, the minimum energy involved would be 0.22 µJ which would result in at least 0.45 W of switching loss if run at 2 MHz. If the device switched a full 200 V with no ZVS at all, it must dissipate 1.42 W even if the load current was zero. Thus the benefits of minimizing the energy integral of the output capacitance are clear. Similarly the output charge integral per (11) is easily computed in closed form as well. The total output charge transfer required to drive an Si7302DN from 0 V to a voltage V_r is simply the area under the curve in figure 15 between the limits 0 and V_r. The required charge Q_{oss} equals:

$$Q_{OSS} = Co \cdot Vr + \frac{Cjo}{(1-m)} \cdot Vj \cdot [(1+\frac{Vr}{Vj})^{1-m} - 1] \quad (15)$$

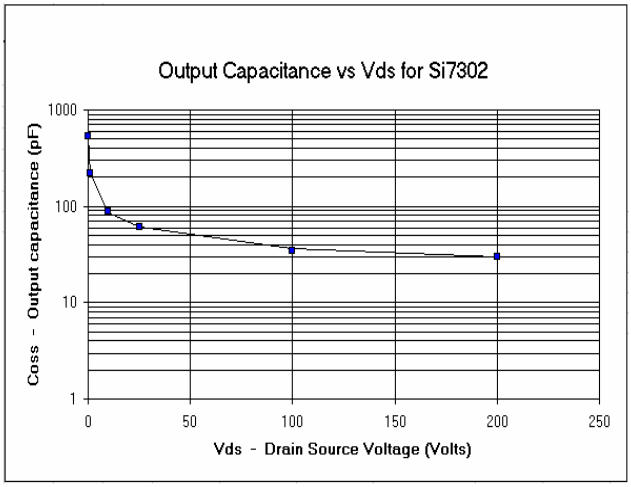


FIGURE 15
MEASURED AND CALCULATED
C_{oss} vs V_{DS} FOR THE Si7302DN

To transition the drain from 0 to V_r = 200 V would require 9.1 nC, making the effective linear output capacitance for switching to 200 V equal to 45.5 pF.

SUMMARY

One difficulty in these figures of merit is that they do not allow for weighting the relative importance of the various parameters. For example a product of $r_{DS(on)}$ and a device capacitance (effective or otherwise) places the same relative importance on both parameters despite the fact there may be cases where the user may wish to weigh the $r_{DS(on)}$ more than the capacitance. For example in consideration of figure 12 and 13, the effect of the output capacitance will be much more significant when a higher voltage is switched, so for offline designs it may be advisable to equally weight the capacitance and the $r_{DS(on)}$. However for some lower-voltage applications, it may be desirable to weight the $r_{DS(on)}$ more than the capacitive derived parameter. With equal weighting for each, the user is evaluating a preferred process because the effect of the die size is eliminated. However, two devices in the same package

may have differing die sizes, equivalent cell densities, etc, so a weighting factor may be useful in determining the appropriate device for a specified package, socket, or footprint. This method quickly becomes much more complicated as other component merits, such as R_g, become increasingly relevant.

A method using weighted logarithms is introduced to consider many other important contributing factors although the relevance of the FOM units must be abandoned in this approach. A way to use different weighting factors for each FOM element can be seen by raising each element in the FOM to a power.

$$FOM = (A^{\alpha}) * (B^{\beta}) * (C^{\chi}) * ..... \quad (16)$$

where A, B, C, etc are the FET parameters relevant to the application and where exponents α, β, χ, etc represent the relative scaling/weighting of each parameter. Taking the natural logarithm of (16):

$$Ln(FOM) = \alpha * Ln(A) + \beta * Ln(B) + \chi * Ln(C) + ... \quad (17)$$

where the weighting introduced by the exponents is more evident.

For example, in the control switch of a buck converter, we might have:

$$Ln(FOM) = Ln(Rdson) + Ln(Qgd) + Ln(Rg) \quad (18)$$

In this example, variations in $r_{DS(on)}$, Q_{gd}, and R_g are given equal weighting, which may not be most desirable in an application. Fortunately, in using the natural log, scaling is easy. Raising each parameter to a power gives it a specific weight. For example:

$$Ln(FOM) = Ln(Rdson) + Ln(Qgd^2) + Ln(Rg^{\frac{1}{2}}) \quad (19)$$

Terms can also be combined in different ways or inverted, and then weighted. For example, to select a device for high dV/dt immunity, for example in a buck rectifier FET, a lower Q_{ratio} and higher gate threshold are needed. Once dV/dt immunity is established, $r_{DS(on)}$on and Q_{rr} can be included as well with weighting factors as deemed appropriate. For example, to skew (weight) the FOM in the direction of high dV/dt immunity (probably at a slight expense to efficiency), one might use:

$$Ln(FOM) = Ln(Rdson^{\frac{4}{8}}) + Ln(Qrr^{\frac{4}{8}}) + Ln((\frac{Qgd}{Qgs})^{\frac{16}{8}}) + Ln((\frac{1}{Vgsth})^{\frac{8}{8}}) \quad (20)$$

This method is quite useful, particularly since there are many parameters relevant to an FOM including, but not necessarily limited to, all the aforementioned parameters plus a device's thermal resistance, thermal capacitance, peak avalanche current rating, single shot avalanche energy, and even cost. The complexity is limited by the information on the datasheet, and the designer's decision to include a weighting factor for each parameter.

REFERENCES

[1] C. P. Schultz, "Power MOSFETs," PCIM Magazine, August 1999, pp. 32-44.

[2] J. Brown, G. Moxey, "Understanding MOSFET Characteristics Associated With The Figure of Merit," Vishay Siliconix AN605, Sept. 2003.

[3] P. Vinciarelli "Optimal Resetting of the Transformer's Core in Single Ended Forward Converters," U.S. Patent 4,441,146 and subsequent reissues.

[4] R. Severns, "dV_{DS}/dt Turn-On in MOSFETs," MOSPOWER Applications Handbook, 1984, Siliconix Inc., chapter 5.4.